CLAIMS

1. A method for reducing variations in noise and temperature in a mixed-signal circuit, the method comprising:

providing memory electrically proximate an analog circuit;

receiving a digital data word at the memory;

determining whether the data word is a desired data word;

performing a dummy write to the memory when the data word is not a desired data word; and

writing the data word to the memory when the data word is a desired data word.

2. The method of claim 1, in which:

the receiving comprises processing an analog input signal and generating the digital data words.

3. The method of claim 1, in which:

the memory comprises dummy memory and acquisition memory;

the performing comprises performing the dummy write to the dummy memory; and

the writing comprises writing the data word to the acquisition memory.

4. The method of claim 1, in which:

the determining comprises:

providing an enable signal having a dummy value and an acquisition value, and

determining whether the enable signal is at the dummy value or the acquisition value;

the performing comprises performing the dummy write to the memory when the enable signal is at the dummy value; and

the writing comprises writing the data word to the memory when the enable signal is at the acquisition value.

5. The method of claim 4, in which:

the memory comprises dummy memory and acquisition memory;

the performing comprises performing the dummy write to the dummy memory; and

the writing comprises writing the data word to the acquisition memory.

6. The method of claim 5, in which the dummy memory comprises no more than a single memory location in the memory.

7. The method of claim 5, in which the dummy memory comprises a range of memory locations in the memory.

8. The method of claim 1, in which:

the memory comprises memory locations corresponding to memory addresses; and

the method additionally comprises initializing a memory address;

the performing comprises performing the dummy write to the memory location indicated by the memory address; and

the writing comprises writing the data word to the memory location indicated by the memory address.

9. The method of claim 8, in which the performing additionally comprises maintaining the same memory address after the dummy write has been performed.

10. The method of claim 8, in which the writing additionally comprises changing the memory address after the data word has been written.

11. The method of claim 8, in which the dummy write comprises writing a dummy data word to the memory location indicated by the memory address.

12. The method of claim 8, in which the dummy write comprises writing the data word that is not a desired data word to the memory location indicated by the memory address.

13. A mixed-signal circuit, comprising:

an analog circuit;

memory electrically proximate to the analog circuit, the memory connected to receive digital data words; and

a memory controller connected to the memory, the memory controller operable to cause the memory to write to the memory each of the data words that is a desired data word and additionally to perform a dummy write to memory for each of the data words that is not a desired data word.

14. The circuit of claim 13, additionally comprising an analog/digital circuit operable to process an analog input signal and to generate the digital data words.

15. The circuit of claim 14, in which the analog/digital circuit comprises an analog-to-digital converter.

16. The circuit of claim 13, in which:

the memory controller is responsive to an enable signal and generates an address signal;

the enable signal has a dummy value when the data word is not a desired data word and an acquisition value when the data word is a desired data word;

the memory comprises dummy memory and acquisition memory, and stores the data word where designated by the address signal; and

the memory controller provides the address signal corresponding to the dummy memory when the enable signal is at the dummy value and provides the address signal corresponding to the acquisition memory when the enable signal is at the acquisition value.

17. The circuit of claim 16, in which the dummy memory comprises a single memory location in the memory.

18. The circuit of claim 16, in which the dummy memory comprises a range of memory locations in the memory.

19. The circuit of claim 13, in which:

the memory controller is responsive to a decimation ratio signal and generates an address signal;

the circuit additionally comprises a decimator operable in response to the decimation ratio signal to generate output data words in response to the data words, the output data words comprising, in a given number of clock cycles, respective dummy data words and a desired data word;

the memory is connected to receive the output data words from the decimator and stores the output data words where designated by the address signal in each of the clock cycles; and

the memory controller is operable to maintain the address signal at one value during the given number of clock cycles.

20. The circuit of claim 19, in which the memory controller is operable to change the address signal after the last of the given number of clock cycles.

21. The circuit of claim 19, in which the memory controller includes the decimator.

22. The circuit of claim 13, in which:

the memory controller generates an address signal;

the memory stores the data word where designated by the address signal in each clock cycle; and

the memory controller is operable to maintain the address signal for a given number of clock cycles and changes the address signal after the given number of clock cycles.